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Amendment under 37 CFR 1.312 dated February 11, 2005
Reply to Notice of Allowance of November 12, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1-20. (Canceled)

21. (Currently Amended) A method for transferring data in an information processing system having a processor bus, a processor coupled to said processor bus, a memory bus, a memory unit coupled to said memory bus, a system bus, a device coupled to said system bus, a data transfer unit coupled to said processor bus and said memory bus and said system bus, said method comprising the steps of:

outputting, by said processor, a data transfer request including an address to said processor bus;

receiving said data transfer request by said data transfer unit that ~~enabled~~enables ~~to~~transfer of data between any arbitrary two of said processor, said main memory and said device via a corresponding two of said processor bus, said memory bus and said system bus;

outputting a signal in order to access the memory unit by said data transfer unit according to said data transfer request output from said processor to said

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memory bus if said address corresponds to an address assigned to said memory

unit,

outputting a signal in order to access the device by said data transfer unit

according to said data transfer request output from said processor to said system

bus if said address corresponds to an address assigned to said device;

receiving said data output from said memory unit or said device; and

outputting said data to said processor by said data transfer unit.

22. (Previously Presented) A method for transferring data in an information

processing system according to claim 21, wherein at least one of said processor bus,

said memory bus and said system bus is an address/data multiplexed bus.

23. (Previously Presented) A method for transferring data in an information

processing system according to claim 21, wherein said device is a disk file controller.

24. (Previously Presented) A method for transferring data in an information

processing system according to claim 21, wherein said device is a controller for

drawing and displaying images.

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25. (Previously Presented) A method for transferring data in an information

processing system according to claim 21, wherein said device is a controller for

networks and communication.

26. (Previously Presented) A method for transferring data in an information

processing system according to claim 21, wherein

each of said processor bus, said memory bus, and said system bus has a

data bus for transferring said data, an address bus for transferring said address, and

a control bus for transferring control signals, and

said data transfer unit includes:

a transfer circuit coupled to said data buses of said processor bus, said

memory bus, and said system bus for transferring said data through said data buses,

and

a control circuit coupled to said address bus of said processor bus for

controlling said transfer circuit in accordance with said address provided from said

processor via said address bus of said processor bus.

27. (Currently Amended) A method for transferring data in an information

processing system having a processor bus, a processor operatively coupled to said

processor bus, a memory bus, a memory unit operatively coupled to said memory

bus, a system bus, a device operatively coupled to said system bus, a data transfer

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unit coupled to said processor bus and said memory bus and said system bus, said

method of comprising the steps of:

outputting, by said processor, a data transfer request including an address to

said processor bus;

receiving said data transfer request by said data transfer unit that

~~enabled~~enables ~~to~~ transfer of data between any arbitrary two of said processor, said

main memory and said device via a corresponding two of said processor bus, said

memory bus and said system bus;

outputting a signal in order to access the memory unit by said data transfer

unit according to said data transfer request output from said processor to said

memory bus if said address corresponds to an address assigned to said memory

unit;

outputting a signal in order to access the device by said data transfer unit

according to said data transfer request output from said processor to said system

bus if said address corresponds to an address assigned to said device;

receiving said data output from said memory unit or said device; and

outputting said data to said processor by said data transfer unit.

28. (Previously Presented) A method for transferring data in an information

processing system according to claim 27, wherein at least one of said processor bus,

said memory bus and said system bus is an address/data multiplexed bus.

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29. (Previously Presented) A method for transferring data in an information

processing system according to claim 27, wherein said device is a disk file controller.

30. (Previously Presented) A method for transferring data in an information

processing system according to claim 27, wherein said device is a controller for

drawing and displaying images.

31. (Previously Presented) A method for transferring data in an information

processing system according to claim 27, wherein said device is a controller for

networks and communication.

32. (Previously Presented) A method for transferring data in an information

processing system according to claim 27, wherein

each of said processor bus, said memory bus, and said system bus has a

data bus for transferring said data, an address bus for transferring said address, and

a control bus for transferring control signals, and said data transfer unit includes:

a transfer circuit coupled to said data buses of said processor bus, said

memory bus, and said system bus for transferring said data through said data buses;

and

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a control circuit coupled to said address bus of said processor bus for

controlling said transfer circuit in accordance with said address provided from said

processor via said address bus of said processor bus.

33. (Currently Amended) A method for transferring data in an information

processing system having a processor bus, a processor operatively coupled to said

processor bus, a memory bus, a memory unit operatively coupled to said memory

bus, a system bus, a device operatively coupled to said system bus, a data transfer

unit coupled to said processor bus and said memory bus and said system bus, said

method comprising the steps of:

outputting, by said processor, a data transfer request including an address to

said processor bus;

receiving said data transfer request by said data transfer unit ~~enabled~~enabling

execution of ~~to execute~~ one of data transfer modes which includes a first mode in

which data is transferred between said processor and said memory unit, a second

mode in which data is transferred between said device and said memory unit, a third

mode in which data is transferred between said processor and said device;

outputting a signal in order to access the memory unit by said data transfer

unit according to said data transfer request output from said processor to said

memory bus if said address corresponds to an address assigned to said memory unit

in said first mode;

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outputting a signal in order to access the device by said data transfer unit

according to said data transfer request output from said processor to said system

bus if said address corresponds to an address assigned to said device in said third

mode;

receiving said data output from said memory unit or said device in said first

mode or third mode; and

outputting said data to said processor by said data transfer unit in said first

mode or third mode.

34. (Previously Presented) A method for transferring data in an information

processing system according to claim 33, wherein at least one of said processor bus,

said memory bus and said system bus is an address/data multiplexed bus.

35. (Previously Presented) A method for transferring data in an information

processing system according to claim 33, wherein said device is a disk file controller.

36. (Previously Presented) A method for transferring data in an information

processing system according to claim 33, wherein said device is a controller for

drawing and displaying images.

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37. (Previously Presented) A method for transferring data in an information

processing system according to claim 33, wherein said device is a controller for

networks and communication.

38. (Previously Presented) A method for transferring data in an information

processing system according to claim 33, wherein

each of said processor bus, said memory bus, and said system bus has a

data bus for transferring said data, an address bus for transferring said address, and

a control bus for transferring control signals, and said data transfer unit includes:

a transfer circuit coupled to said data buses of said processor bus, said

memory bus, and said system bus for transferring said data through said data buses,

and

a control circuit coupled to said address bus of said processor bus for

controlling said transfer circuit in accordance with said address provided from said

processor via said address bus of said processor bus.